PATENT
3672-0162P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Hans Gude GUDESON et al. Conf.:

Appl. No.: 10/659,428 Group: TBA

Filed: September 11, 2003 Examiner: TBA

For: METHOD FOR OPERATING A FERROELECTRIC OR ELECTRET MEMORY DEVICE, AND A DEVICE OF THIS KIND

L E T T E R

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 11, 2004

Sir:

Under the provisions of 35 U.S.C. § 119 and 37 C.F.R. § 1.55(a), the applicant(s) hereby claim(s) the right of priority based on the following application(s):

Country	Application No.	Filed
NORWAY	2002 4335	September 11, 2002

A certified copy of the above-noted application(s) is(are) attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____ #39,491
Michael K. Mutter, #29,680

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

MKM/brs
3672-0162P

Attachment(s)

(Rev. 02/12/2004)

3672-162P
GUDESEN, et al.
10/659,428
9-11-03
BSKB
(703)205-8000

KONGERIKET NORGE
The Kingdom of Norway

Bekreftelse på patentsøknad nr
Certification of patent application no

2002 4335

Det bekreftes herved at vedheftede dokument er nøyaktig utskrift/kopi av ovennevnte søknad, som opprinnelig inngitt 2002.09.11

It is hereby certified that the annexed document is a true copy of the above-mentioned application, as originally filed on 2002.09.11

2003.09.23

Line Reum

Line Reum
Saksbehandler

PATENTSTYRET®
Styret for det industrielle rettsvern

BL. 130 - 5.000 - 01.2001 - Hegro Grafisk AS

Applicant: Thin Film Electronics ASA
P.O.Box 1872 Vika
N-0124 OSLO NORWAY

Inventors: Hans Gude Gudesen
17 Rue Fulton
B-1000 Brussels Belgium

Per-Erik Nordal
Båstadryggen 19
N-1387 Asker Norway

Geirr I. Leistad
Jongsstubben 19
N-1337 Sandvika Norway

Per Bröms
Apelgatan 14
S-582 46 Linköping Sweden

Per Sandström
Stiglötsgatan 13
S-586 46 Linköping Sweden

Mats Johansson
Fanjunkaregatan 49
S-58216 Linköping Sweden

Attorney: Geirr I. Leistad of
Thin Film Electronics ASA
P.O.Box 1872 Vika
N-0124 OSLO NORWAY

Title of the invention: A ferroelectric memory device and method for operating the same

The present invention concerns a method for operating a ferroelectric or electret memory device, wherein the memory device comprises memory cells in the form of a ferroelectric or electret thin-film polarizable material exhibiting hysteresis, particularly a ferroelectric or electret polymer thin film, and a first and a second set of respective parallel electrodes, wherein the electrodes of the first set are provided in substantially orthogonal relationship to the electrodes of the second set, wherein the electrodes of said first and second set are provided in direct or indirect contact with the thin-film material of the memory cells, whereby a polarization state in individual memory cells can be read, refreshed, erased or written by applying appropriate voltages to the individual electrodes of respectively said first and second set of electrodes, wherein the method implements a voltage pulse protocol comprising a read and write/refresh cycle respectively with time sequences of voltage pulses of predetermined amplitudes and lengths, wherein a read cycle comprises applying a set of voltage differences to electrodes of respectively said first and second set of electrodes in case data are read out from the memory cells, and wherein the write/refresh cycle of voltage pulse protocol comprises applying another set of voltage differences to electrodes of respectively said first and second set of electrodes in the case where data are written/refreshed to said memory cells, said sets of voltage differences corresponding to a predefined set of potential levels such that the predefined set of potential levels has at least three separate values.

The invention also concerns a ferroelectric memory device, wherein the memory device is adapted for implementing the method according to any of the claims 1-22, wherein the memory device comprises ferroelectric memory cells in the form of a ferroelectric thin film material, particularly a ferroelectric polymer thin film, wherein said ferroelectric memory cells storing data can be in either one of at least two polarization states when no electric field is applied, wherein a first set and a second set of respective parallel electrodes are provided, wherein the first set of electrodes is provided in substantially orthogonal relationship to the electrodes of the second set, said first set and second set of electrodes contacting the ferroelectric memory cells at opposite surfaces of said ferroelectric thin film and wherein said first set and second set of electrodes are adapted to read, refresh or write said ferroelectric memory cells by applying appropriate voltages thereto, said voltages corresponding to a predefined set of potential levels.

Ferroelectrics are electrically polarizable materials that possess at least two equilibrium orientations of the spontaneous polarization vector in the absence of an external electrical field, and in which the spontaneous polarization vector may be switched between those orientations by an electric field. The memory effect exhibited by materials with such bistable states of remanent polarization can be used in memory applications. One of the polarization states is considered to be a logic "1" and the other state a logic "0". Typical passive matrix-addressing memory applications are implemented by letting two sets of parallel electrodes cross each other, normally in an orthogonal fashion, in order to create a matrix of cross-points that can be individually accessed electrically by selective excitation of the appropriate electrodes from the edge of the matrix. A layer of ferroelectric material is provided between or over the electrode sets such that the capacitor-like structures (functioning as memory cells) are formed in the material between or at the crossings of the electrodes. When applying potential differences between two electrodes, the ferroelectric material in the cell is subjected to an electric field which generates a polarization response generally tracing a hysteresis curve or a portion thereof. By manipulating the direction and the magnitude of the electric field, the memory cell can be left in a desired logic state. The passive addressing of this type of arrangement leads to simplicity of manufacture and a high density of cross-points.

Referring to figure 1, a material with a hysteresis loop 100 changes its polarization direction upon application of an electric field that exceeds the coercive field E_C. The hysteresis loop is shown with the voltage rather than the field along the abscissa axis for reasons of convenience. The voltage is calculated by multiplying the field with the thickness of the ferroelectric material layer. A saturation polarization P_S, is obtained whenever a memory cell is subject to the nominal switching voltage, V_S. However, in practice, partial switching will take place upon application of electric fields below this value. The extent of the partial switching depends on the material properties but repeated application of electric fields, even if lower than the coercive field, will ultimately degrade the remanent polarization states P_r 110 and $-P_r$ 112 to the extent that erroneous read results may occur later on. It is the switching protocol, also known as voltage pulse protocol, that determines the electric fields, by applying voltages to the memory array during read and write operations. A proper switching protocol is needed in order to avoid disturbing other cells when an individual cell in a memory array is read or

written. A multiplicity of voltage pulse protocols have been developed to lessen this effect. A few examples can be found in U.S. Patent No. 3,002,182 (Andersson), U.S. Patent No. 4,169,258 (Tannas Jr.) and the published International Patent Application No. WO 02/05287 (Thompson et al.).

Ferroelectric and electret materials generally exhibit a polarization behaviour dependent on environmental factors and also the addressing history. This may pose a problem when these materials are employed in memory devices that are exposed to different ambient and operating conditions. Particularly the polarization behaviour can be influenced by the ambient temperature to which the ferroelectric material is subjected.

Most ferroelectric or electret materials undergo a structural phase transition from a high-temperature non-ferroelectric phase into a low-temperature ferroelectric phase. This transition occurs at a temperature T_C called the Curie point. Lead titanate zirconate, a popular inorganic ferroelectric material, has a Curie temperature of 360°C. The operating temperature of a ferroelectric memory array is normally significantly lower than this and hence poses fewer and smaller problems, if any. If the ferroelectric material is a polymer, however, an increase in the temperature of the polymer, or an increase in the device working temperature, becomes an important factor of disturbance. Figure 2 demonstrates one possible effect of an increased temperature on the hysteresis curve. The smaller curve represents the ferroelectric properties of a material at a higher temperature. An increased sensitivity to the electric field can be noted since the coercive voltage at a lower temperature, V_{CL}, is higher than the coercive voltage at a higher temperature, V_{CH}. If the electric field applied remains unadjusted in spite of a temperature change, the voltage over non-addressed cross-points would increase the risk of an undesired reversal of the polarization direction. Also the switching speed of a ferroelectric memory material will generally be dependent upon its temperature and increases as the temperature becomes higher.

The well-known fact that the hysteresis curve has a temperature dependency is acknowledged in US Patent No. 5,487,029 (Kuroda). In order to prevent undesired erroneous writing in a ferroelectric memory due to a temperature change, Kuroda states that it is necessary to adjust a write voltage with a negative temperature dependency which corresponds to the temperature

characteristics of the hysteresis curve. To this end Kuroda teaches the use of a voltage generator for providing a write voltage which is stabilized by a zener diode with negative temperature characteristics. The zener diode hence adjusts the write voltage and adapts it to the negative temperature dependency of the ferroelectric capacitors. However, it is a difficult task to tune the characteristics of a zener diode with negative characteristics to the temperature characteristics of the hysteresis curve of a ferroelectric memory material, and Kuroda admits that the temperature compensation may resort to other methods than this, but gives no indication of suitable alternatives.

It should be noted that prior art in this field has been developed in the context of inorganic ceramic ferroelectric materials which typically retain their physical integrity and ferroelectric viability in a temperature range which vastly exceeds that encountered in practical memory devices. An example is lead zirconate titanate, PZT, which has a Curie point at 360°C, above which the spontaneous polarization vanishes. In contrast to this there is an emerging class of memory devices based in ferroelectric organic polymers with Curie and/or melting temperatures below 200°C. These materials offer very considerable advantages in terms of processability, cost, technical flexibility etc., but in certain cases may pose problems due to a change in their electrical characteristics when the temperature varies across the range of specified operating temperatures.

However, from the present applicants' work with ferroelectric memory materials and matrix-addressable ferroelectric memory it has emerged that memory materials in the form of ferroelectric polymers do not change their switching characteristics dependent on the temperature in a straight-forward manner, but that the switching characteristics of ferroelectric polymers can be dependent on changes in their operating temperature in more complicated manner and that a temperature increase not always causes a corresponding increase in the switching speed, as might be expected. In addition it has been found that other environmental factors than the temperature may change the switching speed of the memory material. Such factors may be due to environmental influences including temperature, but not limited to that as e.g. atmospheric humidity, mechanical stresses, electrical stresses as well as the previous addressing history of memory cells made with a ferroelectric polymer influence the ferroelectric behaviour of the memory material. Generally it can be stated that a dynamic memory cell response will be

dependent on a number of factors, and while it is not necessary to isolate the separate contributions from these factors, it is very clear that their overall contribution influences the dynamic aspect of the memory response in some way or other. In order to obviate such influences in an all-inclusive manner, it would be near at hand to monitor a memory cell response to an addressing operation by comparing an instant response with an empirically determined reference response, e.g. one obtained under carefully obtained conditions, and then adjust the parameters of the voltage pulse protocol as applied for addressing operations in a passive matrix addressable memory with a ferroelectric polymer as the memory material.

All voltage pulse protocols as applied to the addressing of passive matrix-addressable ferroelectric memories or electret memories wherein the memory material is a ferroelectric or electret polymer, comprise determined pulse sequences with amplitudes set relative to a reference voltage which may be zero and ranging from this value to an appropriate switching voltage, the selection of which may depend on the memory material in question, but which in any case is higher than the coercive voltage. The actual number of voltage levels prescribed by the voltage pulse protocol may be three or even larger and fractional voltages, i.e. voltage levels intermediate between the switching voltage and e.g. zero voltage, are chosen according to a so-called voltage selection rule and preferably either a half or even better a one-third selection rule is used. The voltage selection rule ensures that non-addressed cells and inactive word lines and bit lines are not subjected to voltages or electric fields larger than those corresponding to the switching voltage V_s and that the activation of word lines and bit lines preferably only involves potential adjustments equal to one of the selected fractional voltages. Actually, it has been shown by the applicant that the average minimum voltage level on any word line and bit line in the memory matrix cannot be less than $V_s/3$ and hence there is nothing to gain from employing voltage selection rules with fractional voltage levels smaller than this, e.g. to use a one-fourth selection rule and so on. Moreover, of course, the voltage pulse protocol also determines the voltage levels to be applied in a timing sequence to the respective active and inactive word and bit lines during an addressing operation and hence this aspect of the voltage pulse protocol shall involve not only the pulse lengths, but also the pulse intervals. Briefly stated, the parameters of voltage pulse protocol would ceteris paribus be determined as said and set for addressing operations. The applicants' investigations have,

however, made clear that a memory cell's response, as measured by an appropriate parameter, e.g. the switching speed or its time derivative, is dynamic and changes in time dependent on the various factors listed above and of which in addition to the addressing history can be of major importance. As stated these include the memory material's actual working temperature which largely can be regarded as ambient temperature given that the device is in thermal equilibrium.

Thus it is a primary object of the present invention to provide a method for eliminating or reducing the problems caused by changes in the hysteresis curve, the coercive voltage, and the switching speed with regard to addressing operations in ferroelectric memory arrays. The primary object hence generally aims at obviating change or drift in the response of ferroelectric memory cell due to environmental influences, addressing history and various stresses induced in the operation of ferroelectric memories, whether the stresses are of electrical mechanical, chemical or thermal nature, or combinations thereof.

It is also an object of the present invention to provide a method for switching speed compensation without using voltage-stabilizing circuitry that are prone to temperature effects and drift. Even more particularly it is an object of the present invention to provide a temperature compensation method applicable to the voltage pulse protocol parameters and which shall be particularly suited for use with polymer ferroelectric memory materials in the form of thin films.

The above-mentioned objects as well as further features and advantages are realized according to the invention with a method which is characterized by steps for

a) determining at least one parameter indicative of a memory cell response to the applied voltage differences,

b) determining at least one correction factor for the voltage pulses as given by the voltage pulse protocol on the basis of said at least one parameter indicative of the memory cells response to the applied voltage differences; and

c) selecting for an adaptation of the voltage pulse protocol at least one of the following pulse protocol parameters, viz. pulse amplitudes, pulse lengths and pulse intervals; and

d) adjusting one or more parameter values of at least one of said selected pulse protocol parameters in accordance with said at least one correction factor, whereby one or more pulse amplitudes, one or more pulse lengths, and one or more pulse intervals are adjusted either separately or in combination in accordance with a detected change in the memory cell response; as well as a ferroelectric memory device which is characterized in comprising means for sensing at least one parameter indicative of the temperature of said ferroelectric memory device; a calibration memory for providing at least one temperature-dependent correction factor, the temperature-dependent correction factor being based on said at least one parameter indicative of the temperature of said ferroelectric memory device; and a set of charge pumps for providing said predefined set of potential levels, said set of charge pumps being adapted for adjusting said predefined set of potential levels in accordance with the at least one temperature-dependent correction factor.

Additional features and advantages of the present invention will be apparent from the appended dependent claims.

The present invention shall now be explained in greater detail by means of a discussion of exemplary embodiments thereof and in conjunction with the appended drawing figures, of which

figure 1 shows as mentioned in the introduction, a schematic hysteresis curve of a ferroelectric memory material;

figure 2 as mentioned in the introduction, a comparison of two hysteresis curves belonging to the same ferroelectric memory material and recorded at different temperatures;

figure 3 a block diagram illustrating a memory circuit according to the preferred embodiments;

figure 4a a principle drawing of a passive matrix addressing arrangement with crossing electrode lines;

figure 4b a principle drawing of a passive matrix with cells containing ferroelectric material localized between the overlap of crossing electrode lines;

figure 5 a read and write voltage switching protocol with four separate potential levels to be controlled on the word lines and bit lines;

figure 6a schematically the magnitudes of the potential levels in a switching protocol as they vary with temperature according to a first preferred embodiment;

figure 6b schematically the magnitudes of the potential levels in a switching protocol as they vary with temperature according to a second preferred embodiment;

figure 6c schematically the magnitudes of the potential levels in a switching protocol as they vary with temperature according to a third preferred embodiment;

figure 7a a block diagram illustrating an analog temperature compensation circuit according to the invention;

figure 7b a block diagram illustrating a digital temperature compensation circuit according to the invention;

figure 8 a block diagram illustrating an extension to the compensation circuits in figs. 7a or 7b for determining an actual switching speed according to the invention, and

figure 9 a passive matrix-addressable device implementing the method according to the invention.

Before the present invention is explained with reference to preferred embodiments a brief review of its general background shall be given with particular reference to the structure of matrix-addressable ferroelectric memories and how they generally are addressed.

With reference to fig. 3, it shows in a simplified block diagram form the structure and/or functional elements of a matrix-addressable ferroelectric memory and as can be adapted for the purposes of the present invention. The memory macro 310 consists of a memory array 300, row and column decoders 32, 302, sense amplifiers 306, data latches 308 and redundant word and bit lines 304, 34. The row and column decoders 32, 302 decode the addresses of memory cells while sensing is performed by the sense amplifiers 306. The data latches 308 hold the data until part or all of the data is transferred to the memory control logic 320. The data read from the memory macro 310 will have a certain bit error rate (BER) which can be decreased by replacing defective word and bit lines in the memory array 300 with

redundant word and bit lines 304, 34. In order to perform error detection the memory macro 310 may have data fields containing error correction code (ECC) information. The memory control logic 320 module provides a digital interface for the memory macro 310 and controls the reads and writes of the memory array 300. Memory initialisation and logic for replacing defective bit and word lines with redundant word and bit lines 304, 34 will be found in the memory control logic 320 as well. The device controller 330 connects the memory control logic 320 to external bus standards. A charge pump mechanism 340 generates some of the voltages needed to read and write the memory cells. A separate clock input, given by the device controller 330 via an oscillator (not shown), will be used by the charge pump mechanism 340 for charge pumping in order to remain independent of the bit rate of the application using the memory macro 310.

As the method according to the present invention applies to the protocols used for addressing the matrix-addressable ferroelectric memory, i.e. protocols applied to operations such as read, reset, erase, write, relevant protocols shall now be explained with reference to the matrix as depicted in fig. 4a, 4b respectively.

It may be useful to review the function of the preferred embodiments in a generalized fashion, with reference to the matrix shown in figures 4a and 4b. In order to conform to standard terminology, it is henceforth referred to the horizontal (row) electrode lines as word lines 400, abbreviated WL and to vertical (column) electrode lines as bit lines 410, abbreviated BL. These reside within e.g. the memory array 300. It is desired to apply a voltage that is sufficiently high to switch a given cell 420, either for defining a given polarization direction in that cell (writing), or for monitoring the preset polarization direction (reading). The ferroelectric material located between the electrodes functions like a ferroelectric capacitor 422. Accordingly, the cell 420 is selected by setting the potentials of the associated word line 402 and bit line 412 (the active lines) such that

$$\Phi_{activeBL} - \Phi_{activeWL} = V_S \qquad (1)$$

At the same time, the numerous word lines 400 and bit lines 410 that cross at cells 420 not addressed must be controlled in potential such that the disturbing voltages at these cells 420 are kept below the threshold for partial switching. Each of these inactive word lines 400 and bit lines 410 crosses the

active word line 402 and active bit line 412 at a non-addressed cell 420. Four distinct classes of cells 420 can be defined in the matrix according to the perceived voltages across the cells 420:

i) $V_i = \Phi_{activeBL} - \Phi_{activeWL}$ (active word line crossing active bit line) (the selected cell),

ii) $V_{ii} = \Phi_{inactiveBL} - \Phi_{activeWL}$ (active word line crossing inactive bit line),

iii) $V_{iii} = \Phi_{activeBL} - \Phi_{inactiveWL}$ (inactive word line crossing active bit line), and

iv) $V_{iv} = \Phi_{inactiveBL} - \Phi_{inactiveWL}$ (inactive word line crossing inactive bit line).

In practical devices where it is desired to minimize cost and complexity, it is of primary interest to focus on the special case where all inactive word lines 400 are at a common potential $\Phi_{inactiveWL}$, and correspondingly all inactive bit lines 410 are at a common potential $\Phi_{inactiveBL}$. By summing the voltages around a closed loop in the matrix grid, the following condition applies, viz.

$$V_i = V_{ii} + V_{iii} - V_{iv} \qquad (2)$$

Given the value of $V_i = V_S$, the minimum voltage value attainable across the non-addressed cells 420 is thus

$$|V_{ii}| = |V_{iii}| = |V_{iv}| = V_S/3 \qquad (3)$$

At least four separate potentials are required to achieve this, i.e. Φ_0, $\Phi_0+V_S/3$, $\Phi_0+2V_S/3$, Φ_0+V_S, where Φ_0 is a reference potential. The potentials must be imposed on the electrodes in the matrix, and any change in potential on one of the electrodes must be coordinated with adjustments in the other potentials such that no cell 420 experiences a voltage exceeding $V_S/3$. In practice, several other factors must be heeded also, e.g. related to minimizing switching transients (charge or discharge currents) and reducing the complexity of the driving circuitry.

There exists other switching protocols as well, e.g. a three-level protocol with $V_S/2$ as the voltage across certain non-addressed cells 420 provided that $V_S/2$ is lower than V_C in that particular case. However, the type of switching protocol used does not limit the invention in any way. The switching protocol shall now be discussed in further detail.

Figure 5 illustrates a four-level switching protocol comprising a read cycle and a write or refresh cycle. It will be clear from the example that no non-addressed cell experiences a voltage exceeding one third of the nominal switching voltage. The time markers, 0 ... 10, indicate different activities in the switching protocol depicted in figure 5. It is assumed below that Φ_0 equals 0 V. These activities will now be described.

t_0 is the quiescent state where all word lines and all bit lines are at two thirds of the nominal switching voltage, $2V_S/3$.

At t_1 the inactive bit lines 410 are adjusted from quiescent value to $V_S/3$. This results in voltages across the cells such that $V_{ii} = V_{iv} = -V_S/3$.

At t_2 the active bit lines 412 are adjusted to VS resulting in $V_i = V_{iii} = V_S/3$. All cross-points now experience an absolute value of one third of the nominal switching voltage. The time delay from t_1 to t_2 is arbitrary and zero or negative timings are acceptable as well.

t_3 is the start of the read delay which lasts until t_4 and wherein the active word line 402 is pulled down to a 0 V potential. V_i now equals V_S thereby enabling the reading of addressed cells. V_{iii} remains at $V_S/3$ while V_{ii} and V_{iv} remain at $-V_S/3$.

At t_4 the read delay has elapsed the active word line is returned to $2V_S/3$ thereby repeating the situation after t_2.

At t_5 all bit lines are returned to the quiescent potential. This step is the reversal of steps t_2 and t_3 taken together. The read cycle has been completed and all word lines and bit lines have returned to the quiescent state similar to t_0.

At t_6 the inactive word lines 400 are lowered from quiescent value to $V_S/3$ as a first step in the write or refresh cycle. This results in voltages across cells such that $V_{iii} = V_{iv} = V_S/3$.

At t_7 the active bit lines which should be written to the logic state "1" are adjusted to 0 V potential while the active bit lines which should remain in the logic state "0" stay at the $2V_S/3$ quiescent potential. Looking only at the write or refresh cycle, active bit lines which should remain in the logic state "0" behave as if they were inactive bit lines, the difference being that during the read cycle they were active bit lines. This is a minor problem of linguistic

character that occurs within the territory of destructive read-out memory systems. This results in voltages across cells such that $V_i^{\text{state "1"}} = -2V_S/3$ while $V_i^{\text{state "0"}} = V_{ii} = 0$ and $V_{iii}^{\text{state "1"}} = -V_S/3$ and finally $V_{iii}^{\text{state "0"}} = V_{iv} = V_S/3$. (It can be seen that $V_i^{\text{state "1"}}$ is now clearly bigger than $V_S/3$ and a switch in polarization direction might have begun. However, this is not a problem since the very same cells are intended to be written in the next step.)

t_8 is the start of the write or refresh delay which lasts until t_9 and wherein the active word line is pulled up to a potential of V_S. $V_i^{\text{state "1"}}$ now equals $-V_S$ thereby enabling the writing or refreshing of the desired cells. $V_i^{\text{state "0"}}$ and V_{ii} = move down to $-V_S/3$ where they join $V_{iii}^{\text{state "1"}}$. $V_{iii}^{\text{state "0"}}$ and V_{iv} are still at $V_S/3$.

At t_9 the write or refresh delay has elapsed and all the bit lines are returned to $2V_S/3$ leading to $V_i = V_{ii} = -V_S/3$ and $V_{iii} = V_{iv} = V_S/3$.

At t_{10} all word lines are returned to the quiescent potential. This step is the reversal of steps t_6 and t_8 taken together. The write or refresh cycle has been completed and all word lines and bit lines have returned to the quiescent state similar to t_0 and t_5.

The switching protocol described in figure 5 can be inverted such that all word lines and all bit lines are at one third of the nominal switching voltage, $V_S/3$, in the quiescent state. The active word lines would be set at V_S during the read cycle and at 0 V during the write or refresh cycle. Likewise, the inactive word lines and the bit lines would be modified in a corresponding manner. Apart from the specific voltage levels, the basic features are similar in all switching protocols regardless of the number of levels, and although four levels are used for describing the preferred embodiments it shall be evident that systems with fewer or more levels can benefit from the invention as well.

In connection with the embodiments of the present invention as applied to switching of voltage pulse protocols discussed in the foregoing, there shall below in order to illuminate central aspects of the present invention discussed exemplary embodiments in relation to a handling the specific problem of a change in the switching properties of a ferroelectric memory materials as the temperature varies.

Particularly this trait is manifest in a decrease in the coercive voltage of field as the temperature increases or generally also in an increase in the switching speed with the temperature, as set forth in the introduction. In the case where the ferroelectric material is a polymer thin film, one has also the problem that it may tend to exhibit less polarization as the Curie point is approached. Moreover, also the previous switching history of the ferroelectric memory material may affect the instantaneous ferroelectric properties, particularly as expressed through the properties of hysteresis loop. Well-known phenomena such as fatigue and imprint which has a detrimental effect on the switching properties of a ferroelectric material may, in case they occur, impart a switching history to the ferroelectric memory material that cannot be neglected when its switching properties at a high temperature shall be considered.

The general solution to the temperature-related increase of the switching speed or the decrease in the coercive voltage of a ferroelectric memory device as proposed by the present invention is to introduce an appropriate temperature compensation in potential levels corresponding to the applied voltage differences in the pulse protocols for addressing in the memory. This presupposes that a temperature of the memory is determined either by direct measurement or by a determination through an indirect method. A direct temperature measurement of the working or operating temperature of a ferroelectric memory device can easily be done by mounting a temperature sensor in the memory circuit or on the memory circuit board, as will be described below. The temperature sensor will then sense the working or environmental temperature of the ferroelectric memory circuit. Ideally the environmental temperature will not necessarily be equated with an actual operating temperature of the memory material itself in an addressing cycle. It is e.g. well-known that the switching of e.g. ferroelectric memory cells of a polymer material may induce thermomechanical stresses in the memory material proper. Particularly in stacked memory architectures as known in the art, both the dissipation of generated heat and the damping of mechanical oscillations can cause problems and at any instant the actual operating temperature of the memory material due to slow heat dissipation, as a matter of fact can be higher than the environmental temperature of the circuit itself. However, it may not be practical to perform a direct sensing of the temperature in the memory layer in the memory material, but as the temperature is related to a switching speed of a memory cell, the switching

speed could be measured in an addressing operation and then a predetermined correlation between the switching speed and the temperature of the memory material could be applied for determining the latter. In the following preferred embodiments which all provide for a temperature compensation of one or more potential levels in the pulse protocols shall be described without specific reference to a particular preferred temperature determination, i.e. the temperature can be measured directly or it can be determined in an indirect manner as set out above.

In a first preferred embodiment, the problem of having an operating temperature relatively close to the Curie point of the ferroelectric material is addressed by implementing a temperature coefficient, $k_S(T)$, for altering the nominal switching voltage, V_S. The four potential levels 600, shown in figure 5 as dash dotted horizontal lines, can be denoted V_1, V_2, V_3 and V_4 as shown in figures 6a-c. It should be clear that V_i, V_{ii}, V_{iii} and V_{iv} are the voltages perceived across the cells 420, while V_1, V_2, V_3 and V_4 are the actual potentials, which means that V_1 equals Φ_0, V_4 equals Φ_0+V_S etc. The temperature coefficient is applied to all the potentials as shown in formulas below.

$$V_4 = \Phi_0 + 3/3 * k_S(T) * V_S \quad (4)$$

$$V_3 = \Phi_0 + 2/3 * k_S(T) * V_S \quad (5)$$

$$V_2 = \Phi_0 + 1/3 * k_S(T) * V_S \quad (6)$$

$$V_1 = \Phi_0 + 0/3 * k_S(T) * V_S \quad (7)$$

The simplest form of temperature coefficient is one which has a linear relationship with the temperature. Figure 6a is an example of such a temperature coefficient which can be written in the $k_S(T) = a+b*T$ format. The potentials compensated for temperature 610 are all on an equal relative distance from each other. Depending on the properties of the ferroelectric material in question the temperature coefficient may have non-linear relationships with the temperature, such as $k_S(T) = a+b*T^{0.9}$ or $k_S(T) = a+b*e^{c*T}$. Another option is to use the difference between the operating temperature and the Curie temperature. These advanced options may become necessary since the difference between the operating temperature and the Curie temperature is much smaller for polymer ferroelectrics. It can be unsafe to only rely upon the negative temperature dependency of a zener

diode as is done in U.S. Patent No. 5,550,770. The mathematical operations for determining the temperature coefficient at any time may be done within the ferroelectric memory device, e.g. in the memory control logic 320, or may have been done outside the ferroelectric memory device and incorporated simply in the form of look-up tables. If the memory device in question is small the look-up tables may be reduced.

In a second preferred embodiment, the problem of having an operating temperature in relative proximity to the Curie point of the ferroelectric material is addressed by introducing an offset voltage to one or more of the potential levels. One example of using offset voltages is given in the published International Patent Application No. WO 02/05287 where a low parasitic current load on the bit line during read operations is achieved by adding an offset voltage to the inactive word lines 400 and inactive bit lines 410. The result is that V_{ii} becomes $V_{ii}+\delta$ and that V_{iii} becomes $V_{iii}-\delta$. However, the magnitude of δ must be selected carefully since the perceived voltage across cells 420 where inactive lines cross active lines, in either combination, becomes greater at certain times thus resulting in an undesired reversal of the polarization direction.

The invention, on the other hand, adds an offset voltage to one or two potential levels. In the formulas below, an offset voltage has been added to V_2 in order to decrease the perceived voltage across cells 420 where inactive word lines 400 cross inactive bit lines 410. Such cross-points constitute the majority of the memory array 300 and helps the most in reducing undesired reversal of the polarization direction although the magnitude of δ must still be selected carefully.

$$V_4 = \Phi_0 + 3/3 * V_S \quad (8)$$

$$V_3 = \Phi_0 + 2/3 * V_S \quad (9)$$

$$V_2 = \Phi_0 + 1/3 * V_S + \delta \quad (10)$$

$$V_1 = \Phi_0 + 0/3 * V_S \quad (11)$$

The added offset voltage 624 is shown in figure 6b where it increases the potential V_2 620 above the dash dotted representation of the original potential 600. Alternatively, there can be a simultaneous reduction of the potential V_3 622 by an offset voltage. Similar to the temperature coefficient

of the first preferred embodiment, the offset voltage may vary with temperature. This is represented in figure 6b by the potential V_3 622. Dissimilar to the first preferred embodiment, the potentials compensated for temperature 620, 622 are not on equal relative distances from each other any longer.

In a third preferred embodiment of the invention, a combination of temperature coefficient and offset voltage is employed. Figure 6c shows the influence of the temperature coefficient as dash dotted potentials 610 while the total effect, with the offset voltage 624 as well, is given by the solid potentials V_2 and V_3 630.

The three preferred embodiments described above may all be provided with circuitry according to figures 7a and 7b wherein a temperature sensor is used for sensing a working of environmental temperature that would be suitable for determining a circuit working temperature. Figure 7a shows an analog temperature compensation circuit 700 that could fit e.g. inside the charge pump mechanism 340. A calibration memory 702 provides information about temperature coefficient and/or offset voltage(s) to a digital-to-analog converter (DAC) 704. Together with input from a temperature sensor 706 the converted information is run through a set of comparators 708, 710, 712. As a result, charge pumps 714, 716, 718 control the potentials V_2, V_3 and V_4. It is customary to connect V_1 to the ground, thereby setting $\Phi_0 = 0$ V.

Figure 7b shows a digital temperature compensation circuit 720 that could also fit e.g. inside the charge pump mechanism 340. Input from the temperature sensor 706 is sent to the calibration memory 702 via an analog-to-digital (ADC) converter 722. Data from the correct address in the calibration memory 702 is provided to the digital-to-analog converter (DAC) 704 and run through the set of comparators 708, 710, 712. Again, charge pumps 714, 716, 718 control the potentials V_2, V_3 and V_4, while V_1 is connected to the ground, thereby setting $\Phi_0 = 0$ V.

The circuits of figures 7a and 7b can be altered to accommodate switching protocols with more or fewer levels as well as switching protocols where Φ_0 does not equal zero. It shall be clear that the number of comparators 708, 710, 712 or charge pumps 714, 716, 718 may vary as a result of the number of levels or whether Φ_0 equals zero or not.

As stated above the three preferred embodiments described above also can be used in conjunction with the indirect determination of a working temperature which in this case would be the actual operating temperature of the memory medium itself during addressing or switching operations. This shall take place by means of an indirect procedure based on measuring the switching speed of memory cells as shall be explained with reference to figure 8.

Figure 8 shows a system for indirect determination of the working temperature of the ferroelectric memory device. Two memory cells 420A;420B are used as reference cells. These reference cells may be located in the memory array 300 or provided on a separate reference memory array. One of the cells is set to a logic "0" and the other cell is set to a logic "1". During operation, both of the reference cells are read out. A level detector 800 continuously subtracts the charge density of the "1" reference cell from the charge density of the "0" reference cell. This type of arrangement has been desribed in the published International Patent Application No. WO 02/05288 (Nordal et al.). The difference between the charge densities increases with time as the read out proceeds. However, the difference between the charge densities is affected by the operating environment as well, i.e. temperature, moisture etc. A comparator 810 compares the difference between the charge densities with a predetermined value and sends a stop signal to a counter 820. The counter 820 started counting when the read out operation started. The time elapsed is then forwarded to the calibration memory 702 in order to determine the operating temperature that corresponds with the time needed for the difference between the charge densities to reach the predetermined level.

Now a fourth embodiment of the invention shall be described in which the adjustment of the voltage pulses as applied in a voltage pulse protocol is not performed on the amplitudes, but on the pulse lengths. The voltage pulse protocol is in other words adjusted in such a way that at least a switching pulse length is reduced in proportion to an increase in the switching speed. This increase could of course be due to a temperature-dependent increase in the switching speed, but generally it can be relied on the switching speed as a parameter of a memory cell's response that is influenced by a result of addressing operation carried out, changes in the memory cell's properties and various environmental factors in addition to the temperature. By reducing for instance the pulse lengths as switching speed increases, a readout signal will

not be seriously diminished at high temperatures while a disturb voltage is reduced. In order to achieve a pulse-length control the memory device must comprise a pulse-length controller, which adjusts the pulse lengths in the voltage pulse protocols and preferably this will be done in response to information of the actual switching speed. As of course the given pulse protocol comprises sequences of pulses with different pulse parameters such as lengths, polarities, pulse intervals, the adjustment of pulse length may vary with the type of pulse used in a given pulse protocol. In practice the adjustment of the pulse length could also be seen as an adjustment of the timing sequence in a pulse protocol or at least a part of this timing sequence, e.g. adjustment of pulse lengths may be combined with adjustments in the pulse intervals, i.e. the time between the different pulses in the protocol. As before adjustments can be made on the basis of the temperature measurements simply by using a sensor as set out above and measuring the temperature directly while the pulse length adjustment is then found by using a look-up table. Probably more preferable the switching speed can be found by addressing and monitoring a reference of test memory cells connected in a matrix the same way as memory cells used for ordinary data storage and the switching speed will then be used as a parameter indicative of the memory cell's response as found by simply carrying out an addressing operation for read operation or addressing operation for the reference memory cells. The advantage of using switching speed is that the change thereof shall incorporate the effect or other factors than the temperature, such as humidity, pressure, mechanical stresses and so on.

With reference to fig. 9 a discussion of a ferroelectric memory device adapted for implementing the method according to the invention shall be given. Some of its component parts have already been discussed in connection with fig. 3 and shall hence only be briefly mentioned. As before the memory matrix 300 comprises memory cells 420 between or at a crossings of word lined WL and bit lines BL in the matrix. The matrix is shown as an m·n matrix, i.e. with m word lines WL and n bit lines BL. On bit lines BL1 and BL2 there are shown two reference memory cells A and B which may be set to respectively the first and the second polarization state, i.e. in other words represent a logical 1 and a logical 0. The reference cell A and B are connected with bit lines BL1 and BL2 and form a part of the memory matrix in the same manner as the other memory cells 420 and hence will be subjected to same disturbing influences or dynamic changes that may

occur in the other memory cells, whether due to addressing operations, environmental factors and so on. The memory cells A and B are addressed in a read operation and the result is detected via a sense amplifier on the output and delivered to the unit 900 for determining a switching speed. The switching speed is output to the calibration memory 702 which has an output connected with a pulse length controller 903, while as before another output is connected to the pulse amplitude controller 904, both controllers 903, 904 of course being connected to the memory control logic 320. The memory device in addition may comprise a temperature sensor 700 for sensing a working temperature of the memory and likewise of course with its output connected to calibration memory 702.

As an optional feature as signal analyser 905 is shown connected with output from the reference memory cells A,B and can be used for carrying out a more sophisticated analysis, of not only the switching speed characteristics, but e.g. also in regard of polarization response characteristics of the memory cells.

The calibration memory will now store the measured reference values, possibly also a history vector for the same referring to addressing and reference operations carried out earlier, and shall moreover derive correction values for either pulse length, or pulse amplitudes, said values being input to the pulse length control 903 or the pulse amplitude controller 904 as is the case. The pulse length will be adjusted by some amount +/-δt, while the pulse amplitudes will similarly be adjusted by an amount δV. It shall be understood that e.g. a pulse generator shall input pulses with determined amplitude and or length with the driver control unit 330 and control parameters deriving from the pulse length controller 903 and the pulse amplitude controller 904 could be applied directly to the pulse generator for applying the actual control values to the amplitude or pulse length or both, as stated, and it is evident that the simultaneous adjustment of both pulse amplitude and pulse length can be performed when the control units 903, 904 are operating synchronized. It shall be understood that the component 900 in fig. 9 will be identical with more or less be similar to the component diagram what is shown in fig. 8, while the calibration memory 702 will be common to either kind of controlling operation. This implies that 903, 904 advantageously both will form part of a pulse generator which adjusts a pulse lengths and pulse amplitudes with correction values as derived in the calibration memory 702.

The pulse length can appropriately be set by applying a timing control as known in the art, while pulse amplitude control can be achieved by means of charge pumps set to adjust the voltage with the control value amounting to $+/-\delta V$ as is the case.

Concerning other component parts of the memory device fig. 9 they shall mimic similar components in fig. 3. However, it is taken for granted that their function in a memory device of this kind will be obvious to persons skilled in the art and hence need not be elaborated further. Finally, it should be noted that an adjustment of the voltage pulse protocol in response to changes in the memory cell response shall serve to reduce disturb (i.e. transient voltages generated by e.g. capacitive couplings in the network) to an addressed memory cell in addressing operation. It should also be noted that similar procedures will serve to obviate the effect of both fatigue and imprint to which a memory cell may be much more prone at a higher switching speed, e.g. ensuing from an increase in the temperature.

CLAIMS

1. A method for operating a ferroelectric or electret memory device, wherein the memory device comprises memory cells in the form of a ferroelectric or electret thin-film polarizable material exhibiting hysteresis, particularly a ferroelectric or electret polymer thin film, and a first and a second set of respective parallel electrodes, wherein the electrodes of the first set are provided in substantially orthogonal relationship to the electrodes of the second set, wherein the electrodes of said first and second set are provided in direct or indirect contact with the thin-film material of the memory cells, whereby a polarization state in individual memory cells can be read, refreshed, erased or written by applying appropriate voltages to the individual electrodes of respectively said first and second set of electrodes, wherein the method implements a voltage pulse protocol comprising a read and write/refresh cycle respectively with time sequences of voltage pulses of predetermined amplitudes and lengths, wherein a read cycle comprises applying a set of voltage differences to electrodes of respectively said first and second set of electrodes in case data are read out from the memory cells, and wherein the write/refresh cycle of voltage pulse protocol comprises applying another set of voltage differences to electrodes of respectively said first and second set of electrodes in the case where data are written/refreshed to said memory cells, said sets of voltage differences corresponding to a predefined set of potential levels such that the predefined set of potential levels has at least three separate values, and wherein the method is characterized by

steps for

a) determining at least one parameter indicative of a memory cell response to the applied voltage differences,

b) determining at least one correction factor for the voltage pulses as given by the voltage pulse protocol on the basis of said at least one parameter indicative of the memory cells response to the applied voltage differences; and

c) selecting for an adaptation of the voltage pulse protocol at least one of the following pulse protocol parameters, viz. pulse amplitudes, pulse lengths and pulse intervals; and

d) adjusting one or more parameter values of at least one of said selected pulse protocol parameters in accordance with said at least one correction factor, whereby one or more pulse amplitudes, one or more pulse lengths, and

one or more pulse intervals are adjusted either separately or in combination in accordance with a detected change in the memory cell response.

2. A method according to claim 1,
characterized by adjusting in any case the values of the pulse amplitude and/or the pulse length of a switching voltage pulse in the voltage pulse protocol.

3. A method according to claim 1,
characterized by determining said at least one parameter indicative of a response to the applied voltages in step a) by determining at least one parameter indicative of a switching speed of said ferroelectric memory, and by determining said at least one correction factor in step b) by determining a switching speed-dependent correction factor.

4. A method according to claim 3,
characterized by determining said at least one parameter indicative of the switching speed in step a) by measuring an instantaneous switching speed of said ferroelectric memory.

5. A method according to claim 4,
characterized by measuring said switching speed by measuring the switching speed of one or more reference memory cells.

6. A method according to claim 4,
characterized by measuring said switching speed by analysing ongoing addressing operations including a switching of memory cells in the ferroelectric memory device.

7. A method according to claim 3,
characterized by determining a switching speed-dependent correction factor in step b) by a calculation.

8. A method according to claim 3,
characterized by determining a switching speed-dependent correction factor in step b) by a reading of a look-up table.

9. A method according to claim 3,
characterized by determining a first and a second switching speed-dependent correction factor in step b).

10. A method according to claim 4,
characterized by continuously monitoring the switching speed of the ferroelectric memory device, applying at least one switching speed-dependent correction factor to the voltage pulse protocol implementing the applied voltage differences, adapting the voltage pulse protocol in real time to a change in the response to the applied voltage differences, and applying said real time-adapted voltage pulse protocol for adjusting at least one of the parameter values of the pulse protocol parameters in step d).

11. A method according to claim 10,
characterized by adjusting all parameter values of at least one of the pulse protocol parameters in step d).

12. A method according to claim 1,
characterized by determining said at least one parameter indicative of a response to the applied voltage differences in step a) taking place by determining at least one parameter indicative of the temperature of said ferroelectric memory, and by determining said at least one correction factor in step b) by determining at least one temperature-dependent correction factor.

13. A method according to claim 12,
characterized by determining said at least one parameter indicative of the temperature in step a) by sensing a working temperature of said ferroelectric memory device directly.

14. A method according to claim 12,
characterized by determining a temperature-dependent correction factor in step b) by a calculation.

15. A method according to claim 12,
characterized by determining a temperature-dependent correction factor in step b) by a reading of a look-up table.

16. A method according to claim 12,
characterized by determining a first and a second temperature-dependent correction factor in step b).

17. A method according to claim 16,
characterized by determining the first temperature-dependent correction

factor as a temperature coefficient, said temperature coefficient being applied for adjusting all parameter values of at least one of the pulse protocol parameters in step d).

18. A method according to claim 16,
characterized by determining the second temperature-dependent correction factor as an offset voltage, said offset voltage being applied for adjusting at least one amplitude value or potential level in step d).

19. A method according to claim 16,
characterized by adjusting parameter values in step d) by first performing a first adjustment in accordance with the first temperature-dependent correction factor and thereafter performing a second adjustment in accordance with the second temperature-dependent correction factor, or alternatively performing a first adjustment in accordance with the second temperature-dependent correction factor followed by a second adjustment in accordance with the first temperature-dependent correction factor.

20. A method according to claim 1,
characterized by determining said least one parameter indicative of a response to the applied voltages in step a) by determining at least one parameter indicative of the temperature of said ferroelectric memory device by measuring a switching speed of memory cells in the ferroelectric memory device and applying a predetermined correlation between the measured switching speed and the actual temperature of the ferroelectric memory material of the cells for determining the latter.

21. A method according to claim 20,
characterized by measuring said switching speed by measuring the switching speed of one or more reference memory cells.

22. A method according to claim 20,
characterized by measuring said switching speed taking place by analysing ongoing addressing operations inducing a switching of memory cells in the ferroelectric memory device.

23. A ferroelectric memory device, wherein the memory device comprises ferroelectric memory cells in the form of a ferroelectric thin film material, particularly a ferroelectric polymer thin film, wherein said ferroelectric memory cells storing data can be in either one of at least two polarization

states when no electric field is applied, wherein a first set and a second set of respective parallel electrodes are provided, wherein the first set of electrodes is provided in substantially orthogonal relationship to the electrodes of the second set, said first set and second set of electrodes contacting the ferroelectric memory cells at opposite surfaces of said ferroelectric thin film, and wherein said ferroelectric memory cells by applying appropriate voltages thereto, said voltages corresponding to a predefined set of potential levels; and wherein the ferroelectric memory device is characterized in comprising a means for determining at least one parameter indicative of a response to the applied voltage differences;
a calibration memory for providing at least one correction factor dependent of the determining parameter, the correction factor being based on said at least one parameter indicative of the operating condition of said ferroelectric memory device; and
a set of charge pumps for providing said predefined set of potential levels, said set of charge pumps being adapted for adjusting said predefined set of potential levels in accordance with the at least one correction factor.

24. A ferroelectric memory device of claim 23,
characterized in that said temperature sensor, said calibration memory and said set of charge pumps are all located within a temperature compensation circuit.

25. A ferroelectric memory device of claim 24,
characterized in that the temperature compensation circuit is an analog circuit.

26. A ferroelectric memory device of claim 25,
characterized in that the temperature compensation circuit is a digital circuit.

ABSTRACT

In a method for operating a matrix-addressable ferroelectric memory device a first plurality of voltage differences is applied across a first and a second set of electrodes in a matrix-addressable array when data are read from the ferroelectric memory cells thereof, and a second plurality of voltage differences is applied across the first and the second set of electrodes in the case where data are refreshed or rewritten to the ferroelectric memory cells. In each case the first and second plurality of voltage differences correspond to predefined sets of potential levels. At least one parameter indicative of the temperature of the memory device is determined and used for determining at least one temperature-dependent correction factor for the potential levels, whereby at least one of these levels are adjusted in accordance with the at least one temperature-dependent correction factor.

A ferroelectric memory for implementing the above method comprises means for determining the least one parameter indicative of the temperature of the memory device. This means can either be a temperature sensor or a switching speed sensor which in any case may be provided in a temperature compensation circuit.

Figs. 7a, 8

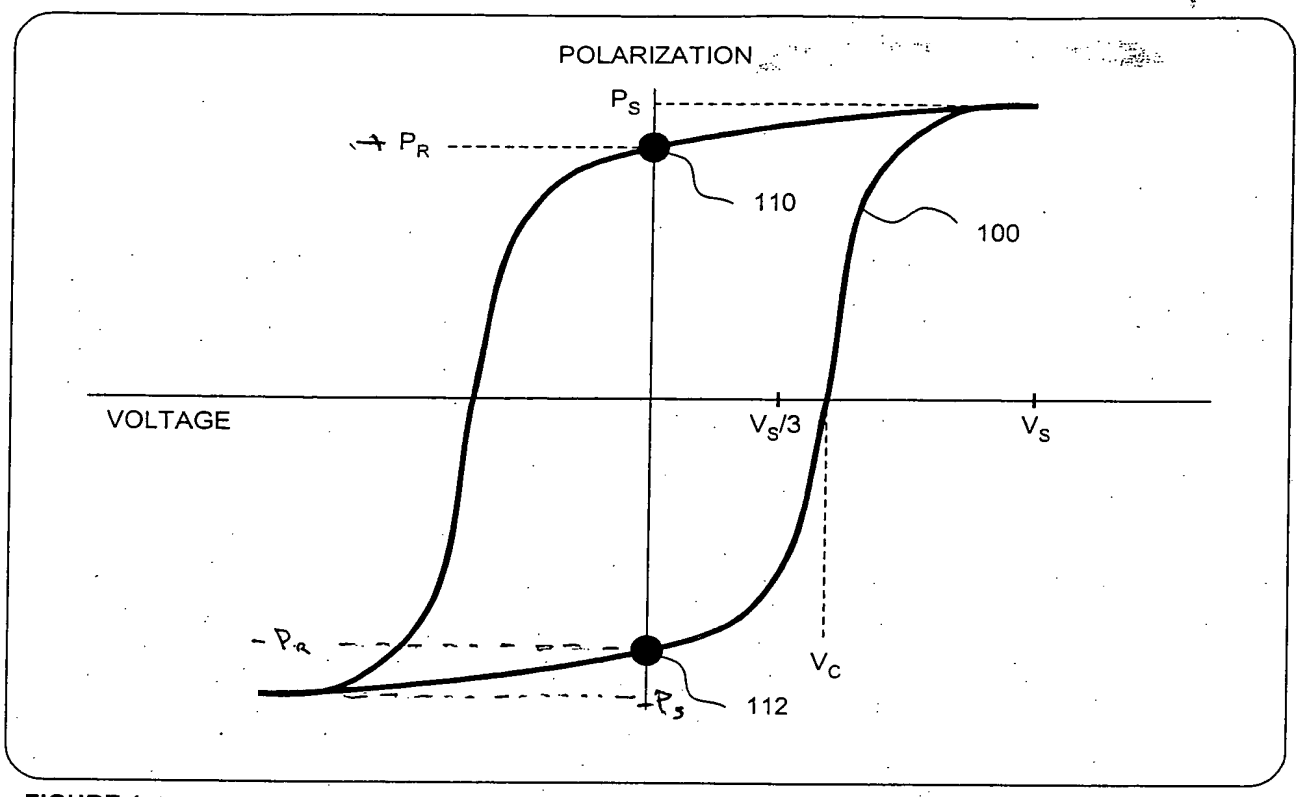

FIGURE 1

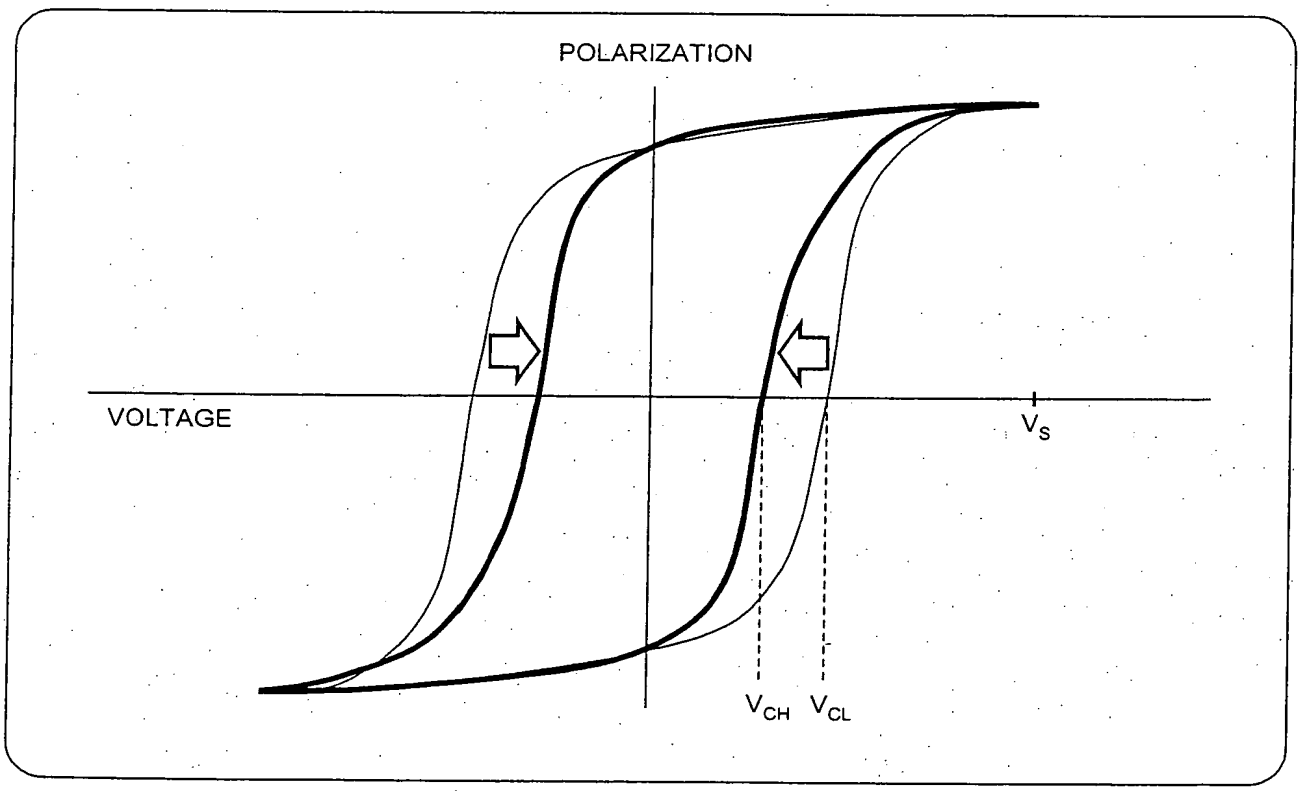

FIGURE 2

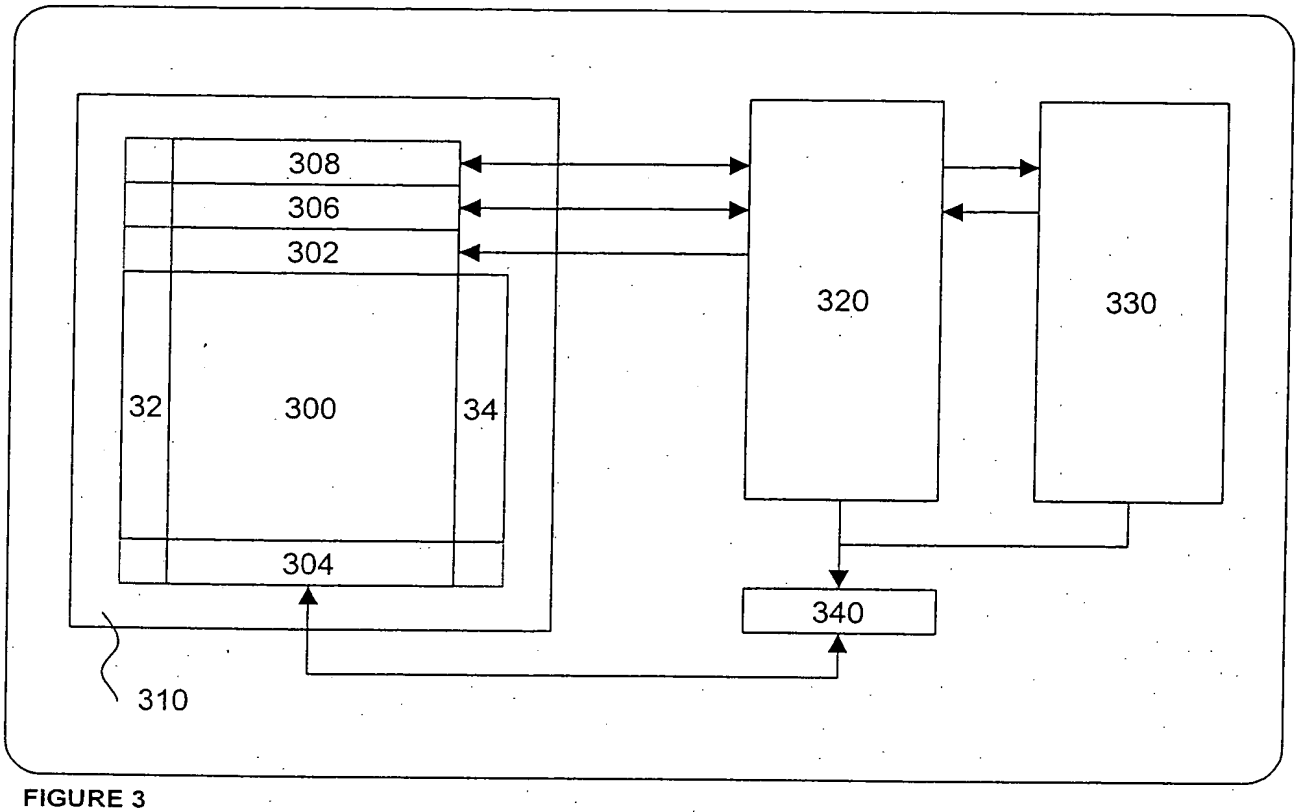

FIGURE 3

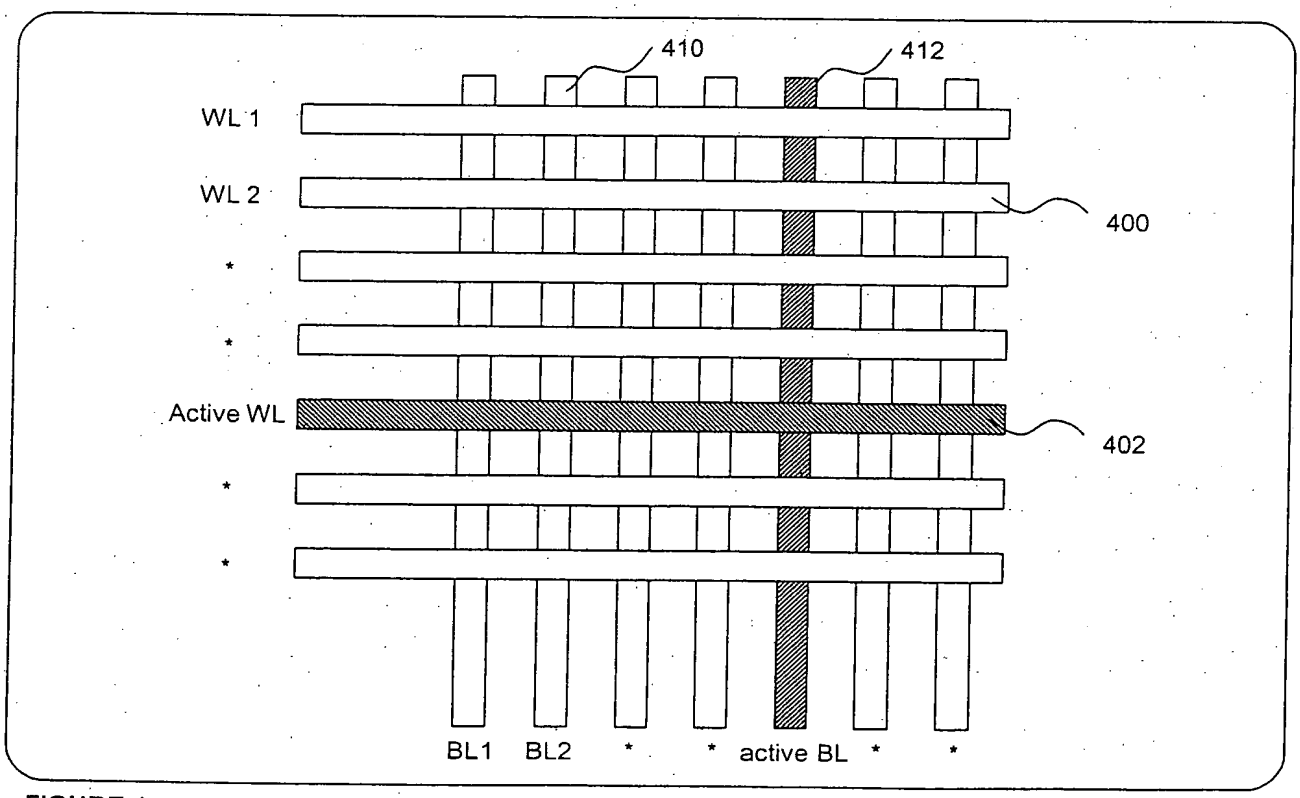

FIGURE 4a

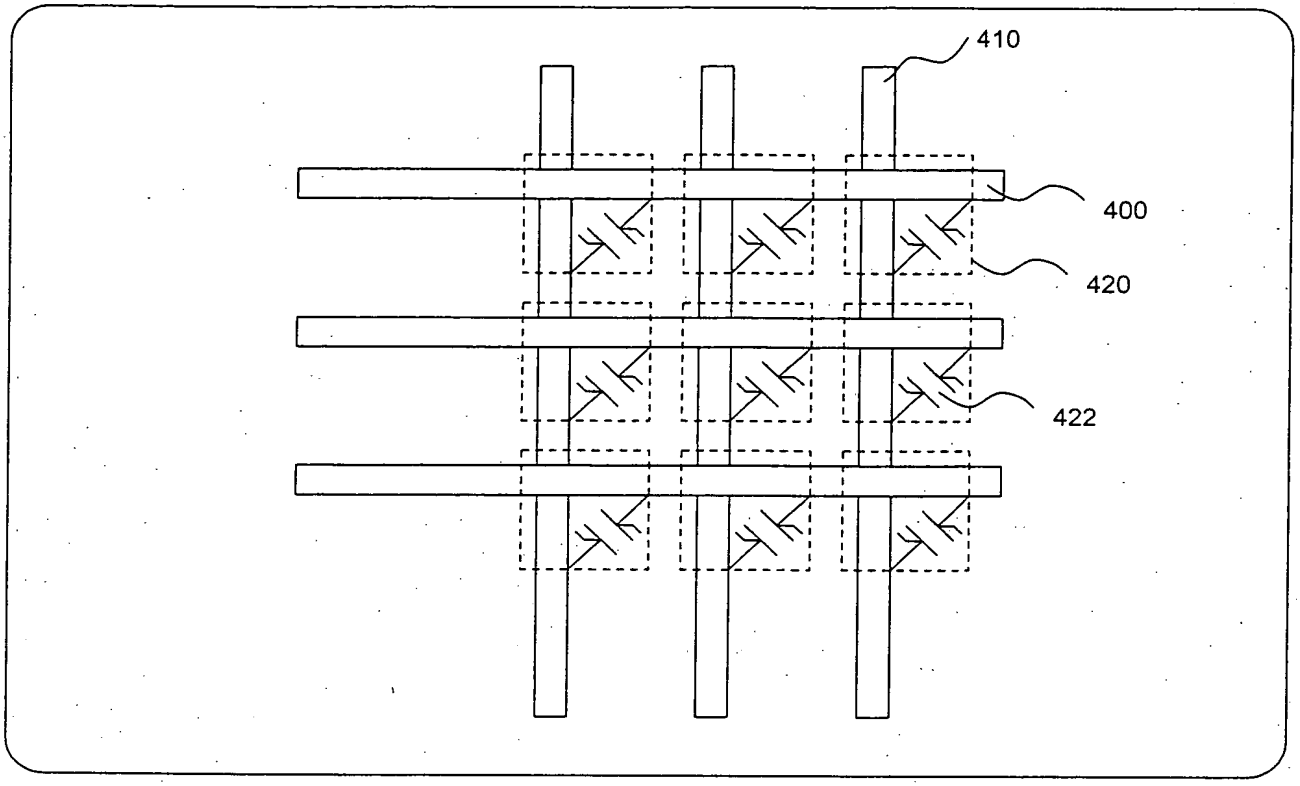

FIGURE 4b

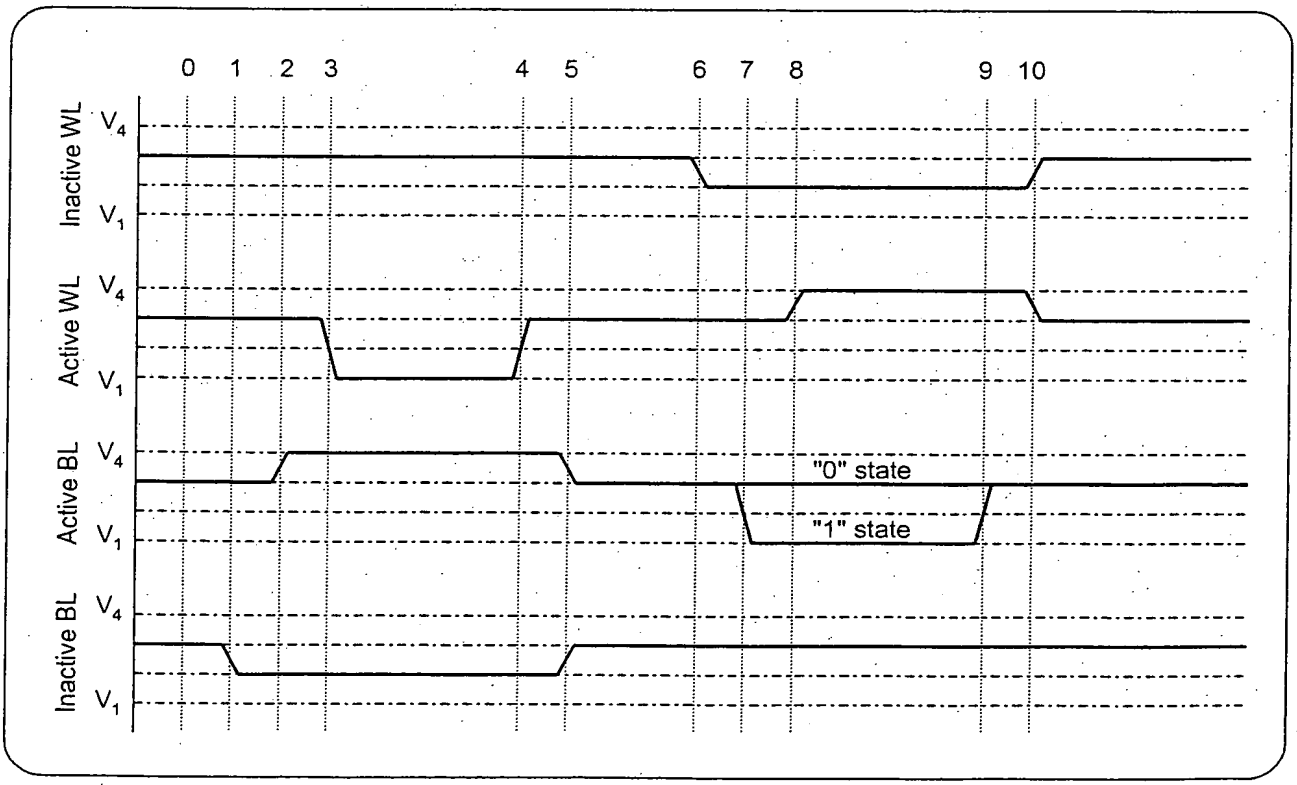

FIGURE 5

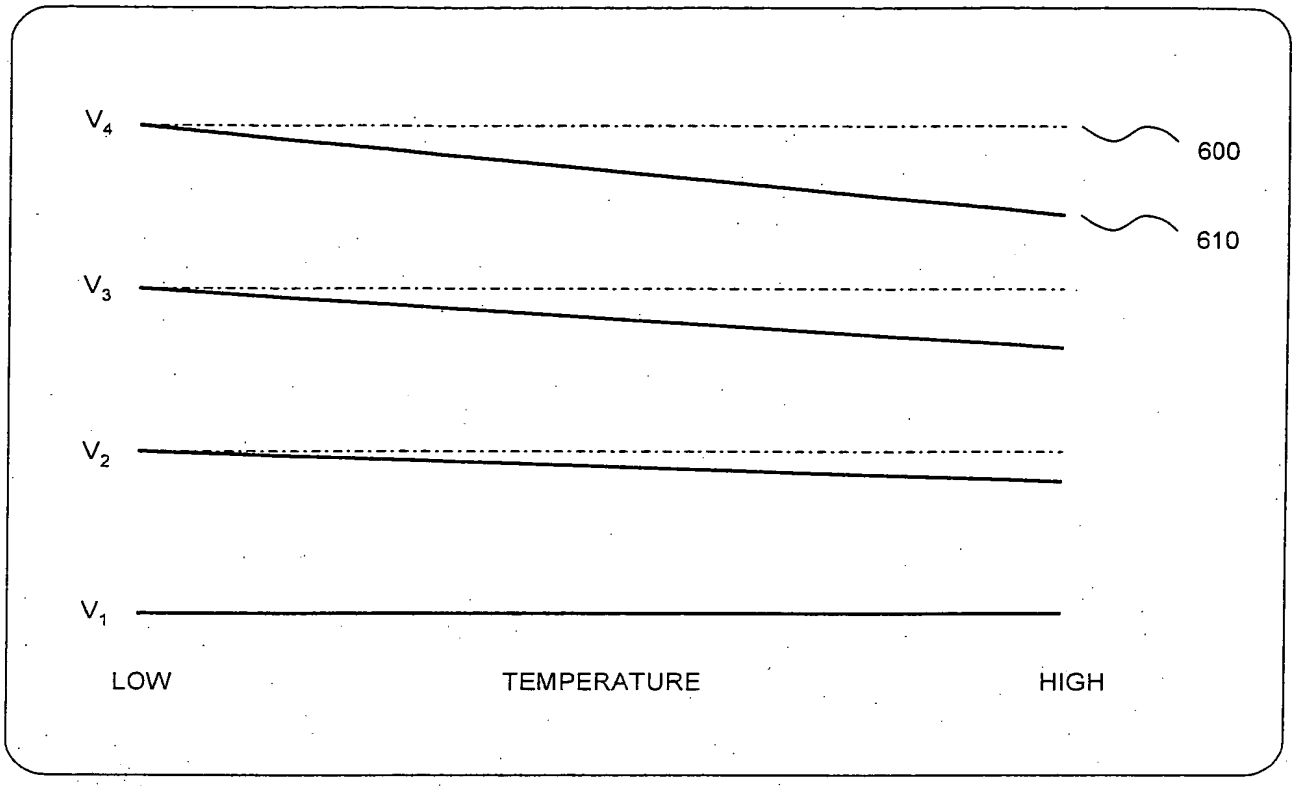

FIGURE 6a

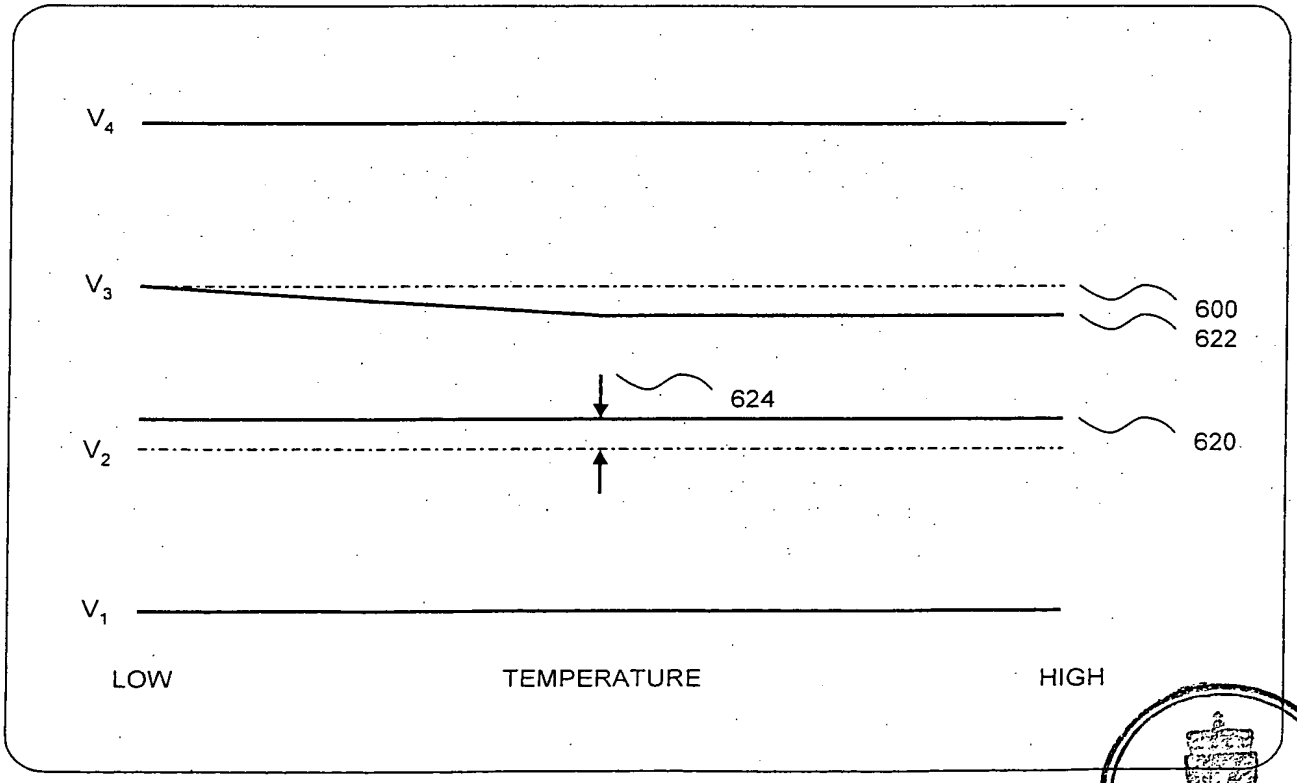

FIGURE 6b

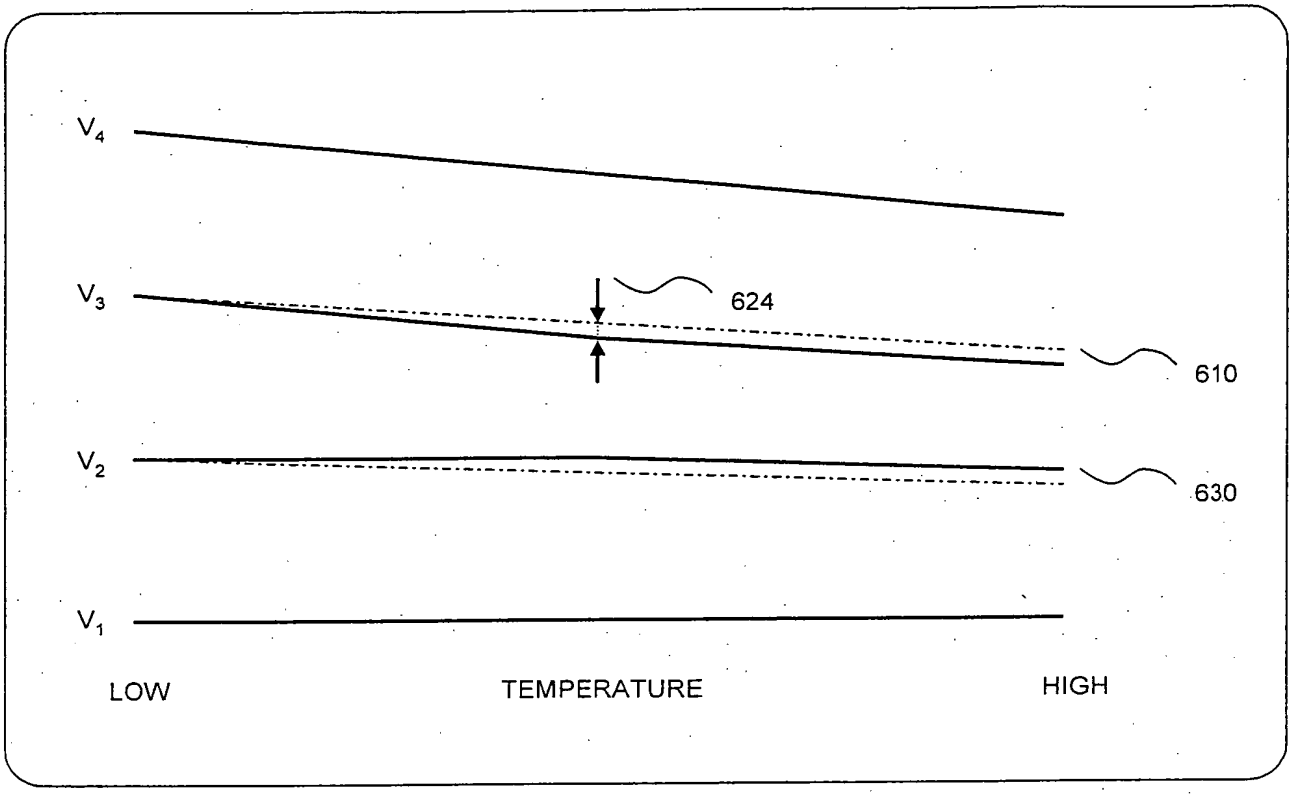

FIGURE 6c

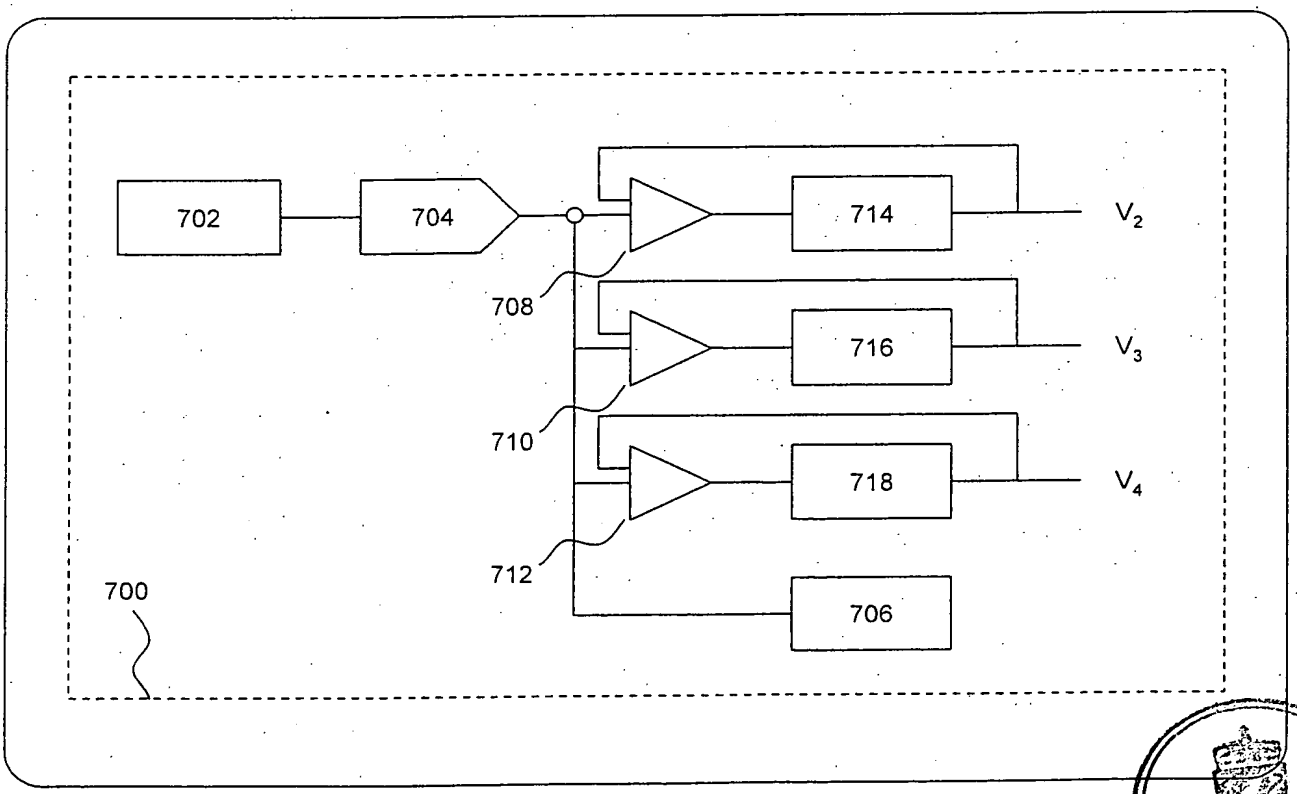

FIGURE 7a

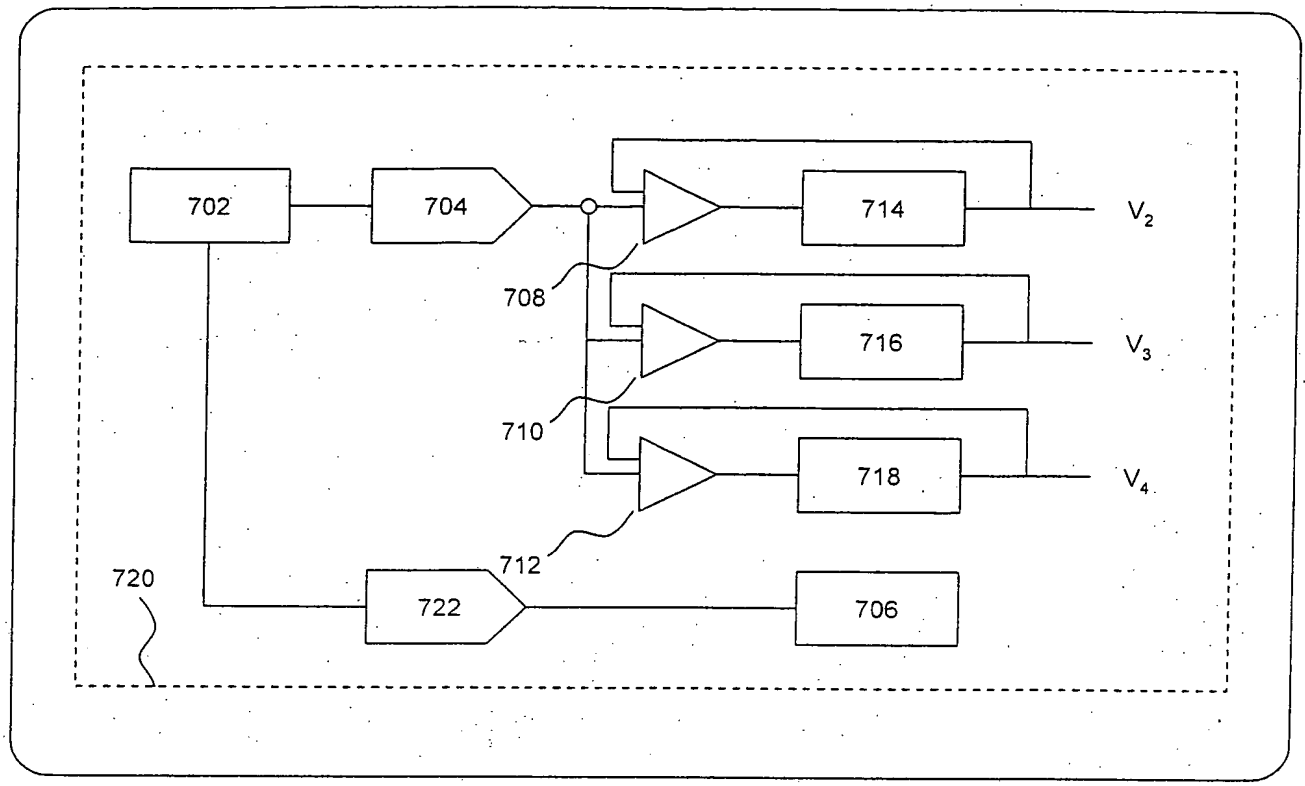

FIGURE 7b

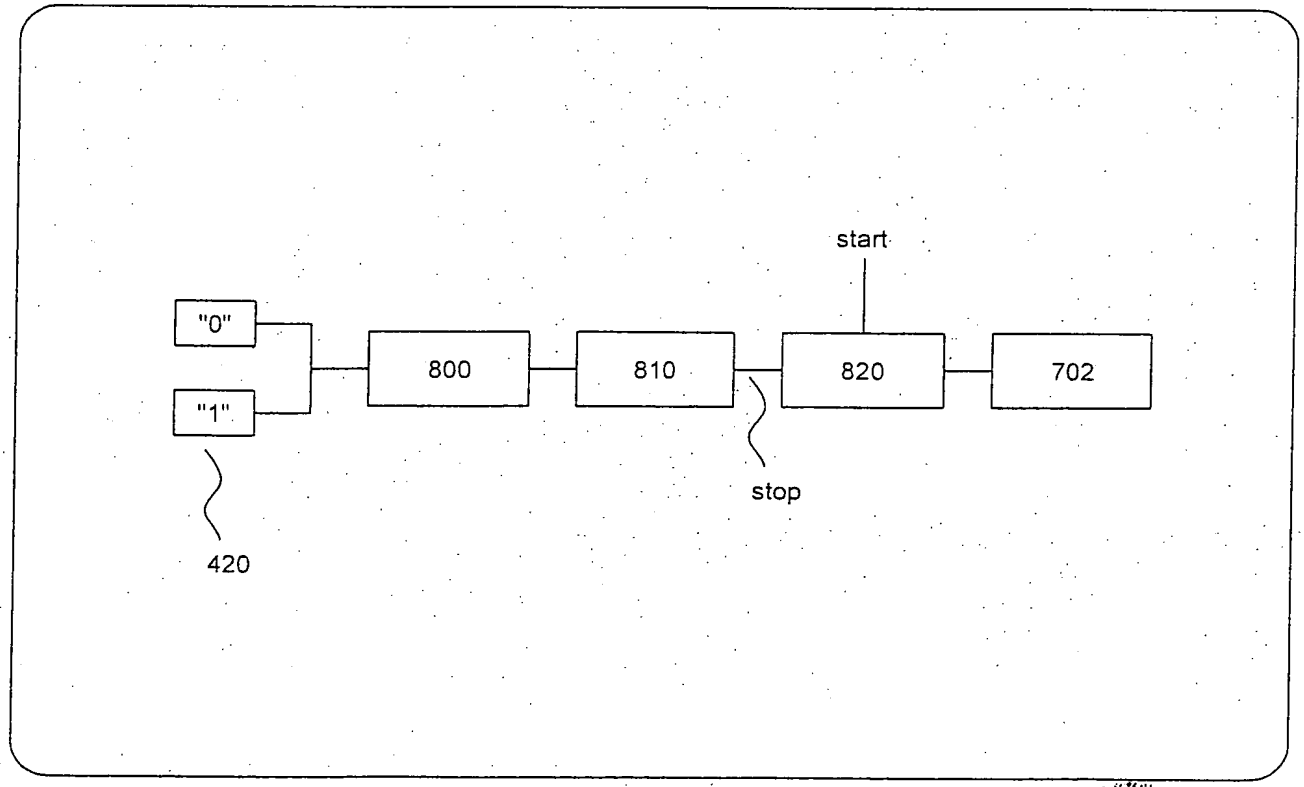

FIGURE 8

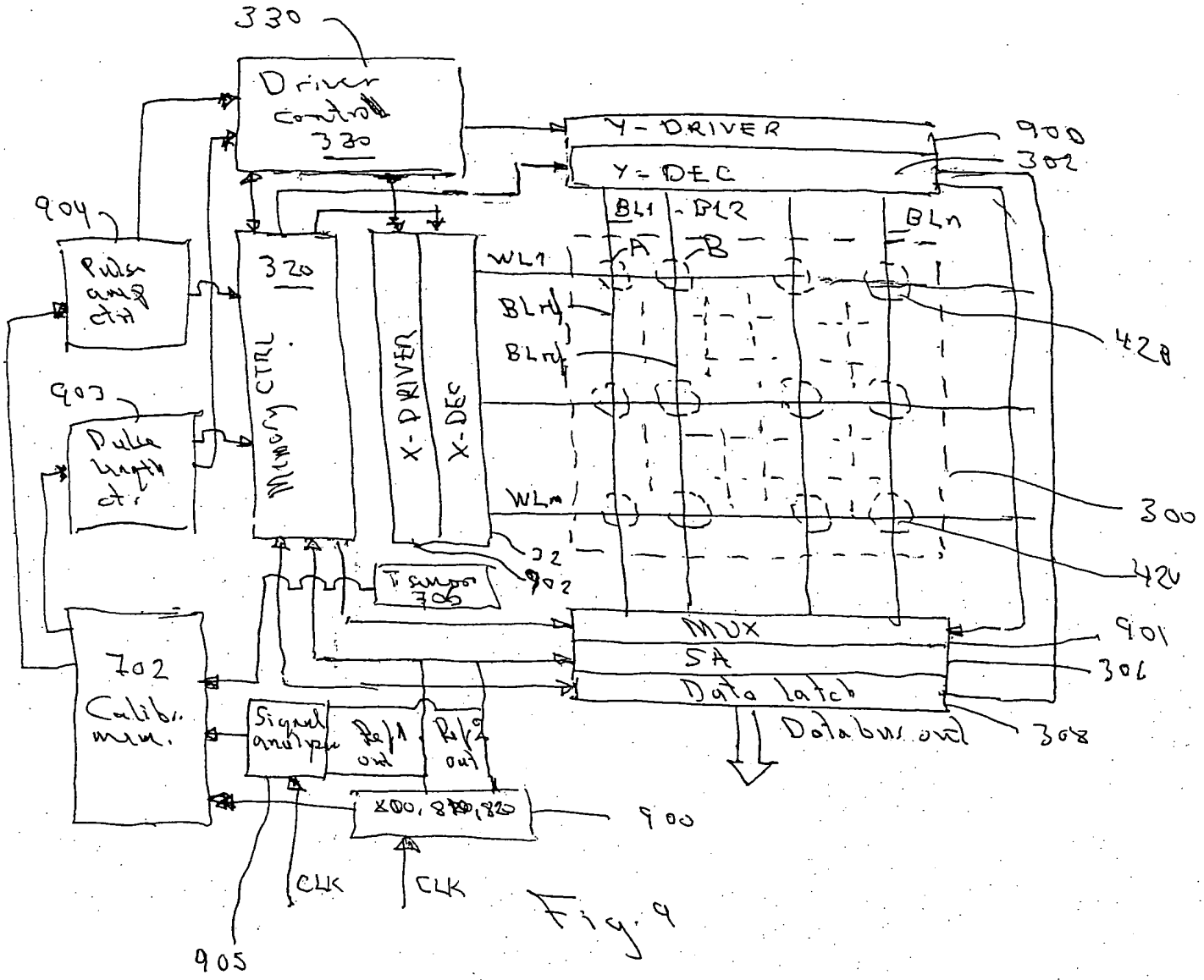

Fig. 9